THERMAL NOISE ESTIMATION IN SWITCHED-CAPACITOR CIRCUITS

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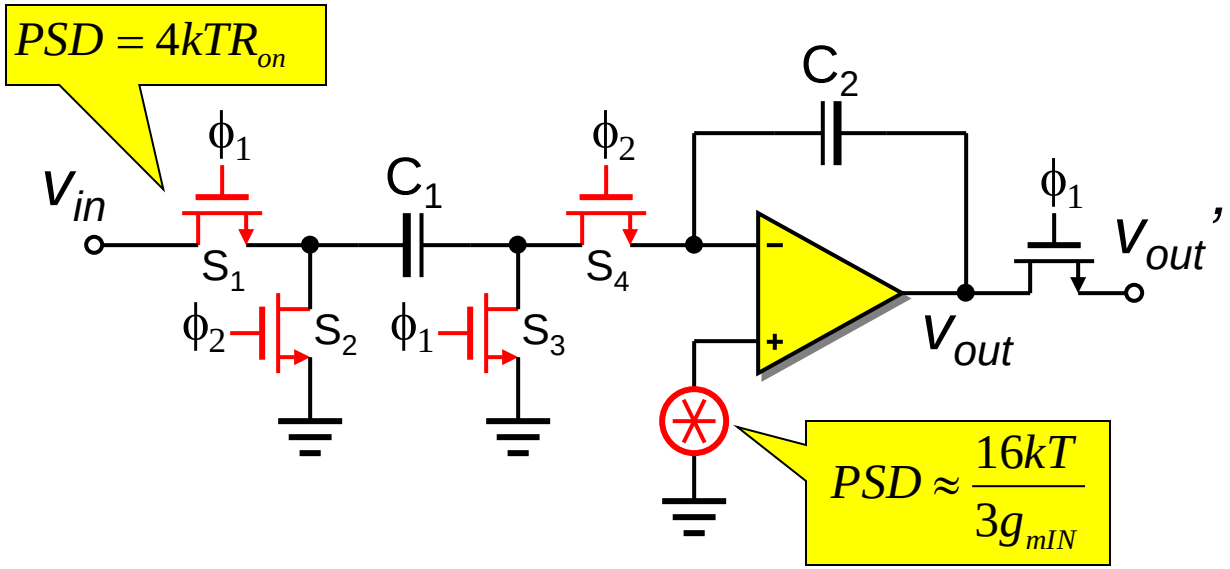
Outline

- Thermal noise effects in an SC integrator
  - Switch (kT/C) noise
  - Opamp thermal noise
- Noise calculations in $\Delta\Sigma$ ADCs
- Noise calculation Example

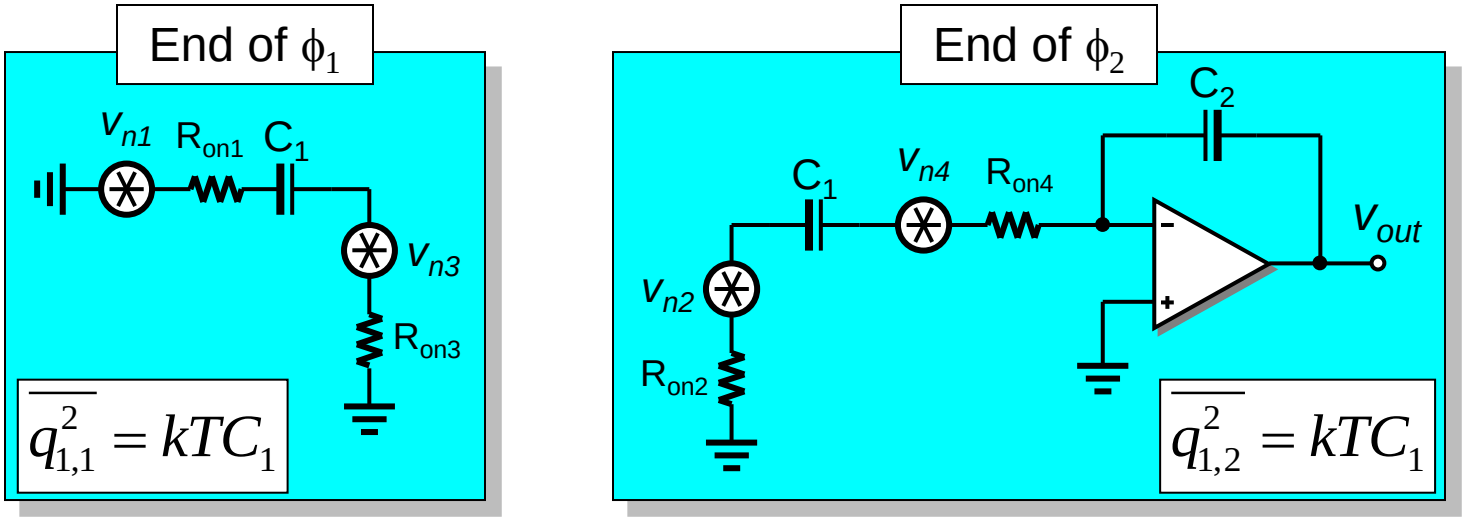
Noise Effects In SC Integrators

- The thermal noise sources are the switches and the opamp.
- Flicker noise is negligible if $f_{corner} << f_s$. If not, techniques such as correlated double sampling or chopper stabilization can be used.



Switch Noise

- Noise charge power in C_1 (assuming ideal opamp):



- MS noise charge into C_2, in every clock period:

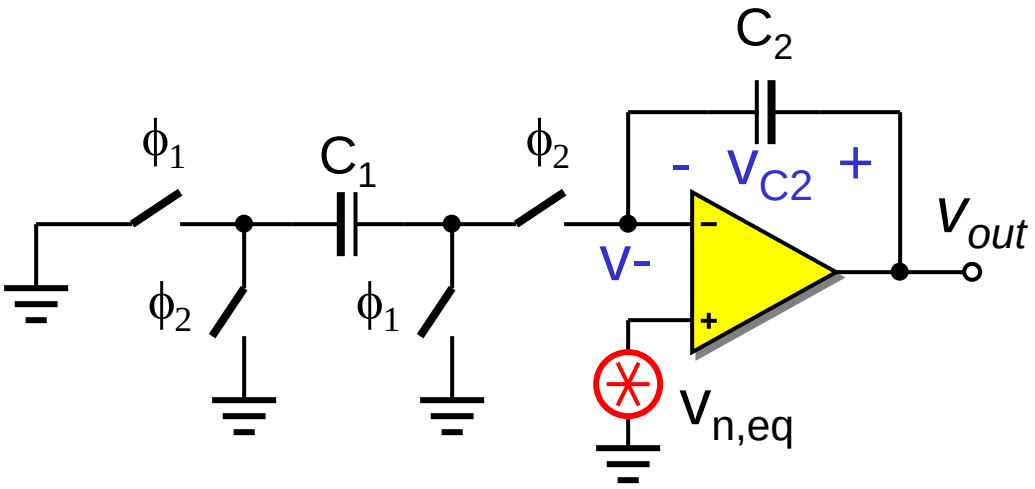
$$\overline{q_1^2} = \overline{q_{1,1}^2} + \overline{q_{1,2}^2} = 2kTC_1$$

- This can be represented by an equivalent input voltage noise source v_{n1} with MS value:

$$\overline{v_{n1}^2} = \frac{2kT}{C_1}$$

Op-amp Noise (1)

- Simplified method, ignoring switch resistance during Φ_2=1



- Charge drawn by C_1 from C_2 in every clock period: C_1 v-. This effect can be represented by equivalent input noise source v_{n2} = v-

Opamp Noise (2)

- To find v-, assume a single-pole model for the op-amp with $\omega_u = g_{m1}/C_L$
- Output MS voltage noise:
  - MS voltage noise of *v*-, by voltage division:

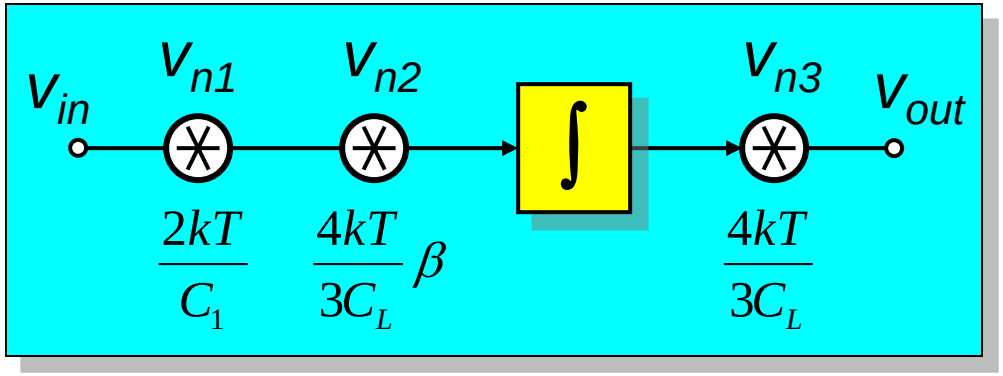
$$\overline{v_{out}^2} = \frac{4kT}{3C_L}\left(1+\frac{C_1}{C_2}\right) \qquad \overline{v_-^2} = \frac{4kT}{3\left(1+C_1/C_2\right)C_L}$$

- C_1 will extract a charge $C_1 v$- from C_2 in every clock period. This effect can be represented by an input source v_{n2}.
- Since $v_{out} = v- + v_{C2}$, an output equivalent source v_{n3} is also required. It represents the unity-gain output noise during $\Phi_1=1$
- Using $\beta = 1/(1+C_1/C_2)$ as the feedback factor:

$$\overline{v_{n2}^2} = \frac{4kT}{3C_L}\beta \qquad \overline{v_{n3}^2} = \frac{4kT}{3C_L}$$

Integrator Noise Model

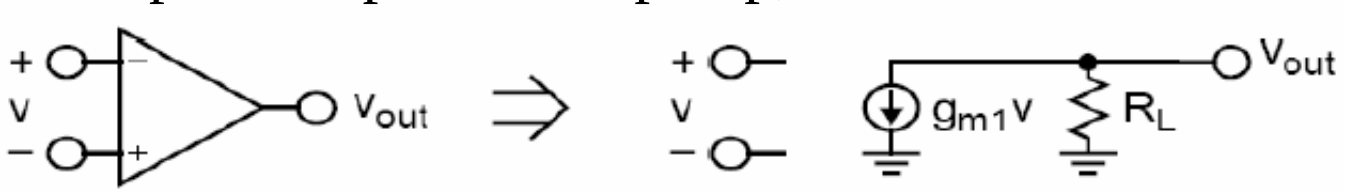
- Combining the effects of switch and opamp thermal noise:



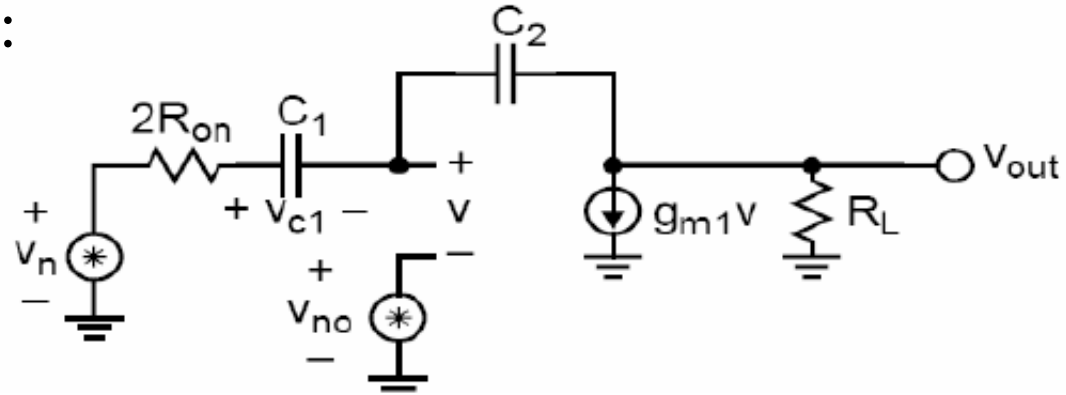
- Insert these noise sources into every integrator and SC branch.

More Accurate Model

Assuming an output-compensated opamp,



During Φ2 :



Noise power acquired by C_1 during Φ_2=1:

From R_{on} : $\dfrac{kTC_1}{1+1/x}$, from v_{no} : $\dfrac{4}{3}\dfrac{kTC_1}{x+1}, x \triangleq 2R_{on}g_{m1}$

Total power acquired in Φ_1 and Φ_2: $\overline{q_1^2} = 2kTC_1(1+\dfrac{1/6}{x+1})$

Design Considerations

- The input – referred noise voltage $\overline{v^2}_{c1} = \overline{q^2}_1 / C^2_1$ is minimized for $g_{m1} >> 1 / R_{on}$. This costs added power. For $g_{m1} << 1 / R_{on}$, the noise power is only 7/6 ~ 1.17 times larger.

- For several input capacitors, the noise charge powers add. For two C1 branches, there is a 3 dB noise increase.

- In the model, now $\overline{v_{n2}^2} = \dfrac{kT / 3C_1}{x+1}$ .The other two sources remain unchanged. The overall input-referred noise is now about 2dB lower than that obtained from the simpler model.

An Efficient Design Algorithm

From previous relations, at the end of $\Phi_2 = 1$,

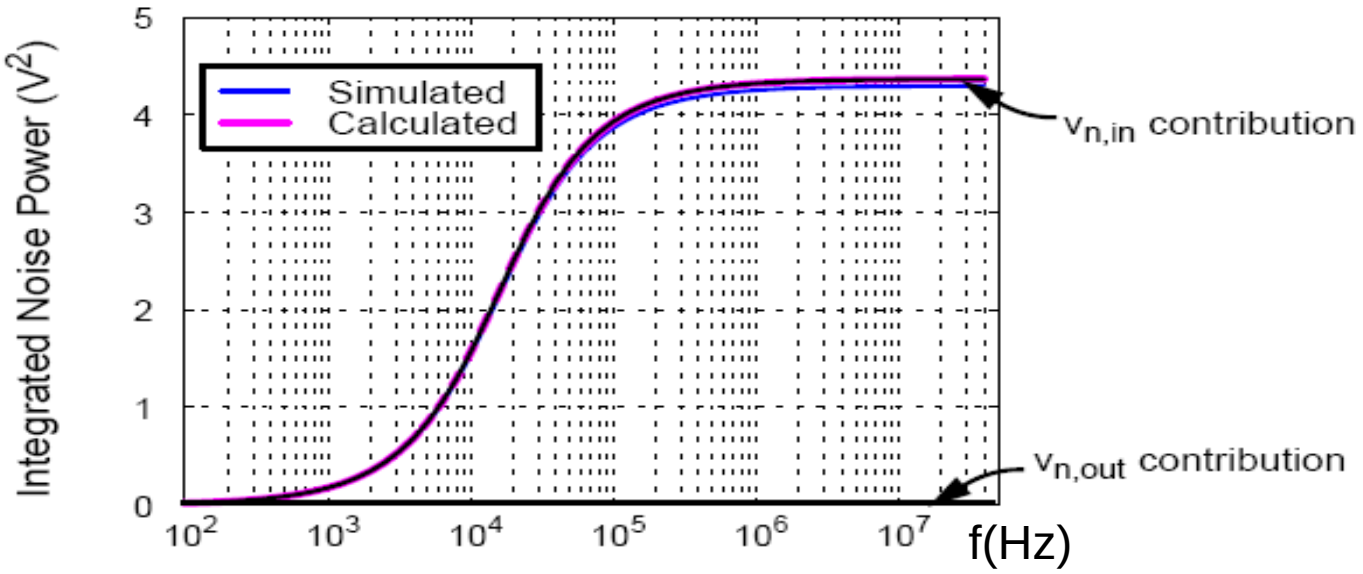
$$gm1 = \frac{kT}{\tau \bar{v}_{c1}^2}(7/3 + 2x) \quad \text{,where } \tau = (2R_{on} + 1/g_{m1})C_1$$

is the settling time constant of the stage, and $\bar{v}_{c1}^2$ is the input-referred noise power .To minimize g_{m1} ,

1. Choose $\tau = [(2\ln 2)(N+1) f_s]^{-1}$, the largest value allowed for settling to N-bit accuracy;
2. Choose $\bar{v}_{c1}^2 = 2^{-(N+1)} \bar{v}_{in,eff}^2$;
3. Choose $x = 2R_{on} g_{m1} << 1$
4. Find g_{m1} and R_{on} from eqs. above;
5. Find C_1 from $C_1 = g_{m1}\tau/(1+x)$

Example (Integrator)

- Let $C_1 = C_2 = 2CL = 1$ pF, $g_{m1} = 4$ mA / V, $R_L = 250k\Omega$, $2R_{on} = 0.5k\Omega$, fs = 100MHz. Then $2R_{on}\, C_1 = C_0 / (\beta g_{m1}) = 0.5$ns $= 1 / 20$fs , allowing for accurate settling.
- Integrating the output noise PSD over 0 to $f_B = f_s / (2 \cdot OSR)$ gives



Calculated and simulated integrated noise powers at the output of the integrator. Simulation used [7].

Noise Calculations in ΔΣ ADCs

- **Step 1:** Identify noise sources in the topology.
- **Step 2:** Calculate PSDs of noise sources.
- **Step 3:** Calculate transfer function from each noise source to output.
- **Step 4:** Integrate each noise PSD over desired bandwidth.

$$\overline{v_{oj}^2} = \frac{2}{f_s} \int_0^{\frac{f_s}{2OSR}} \overline{v_j^2} \cdot \left| NTF_j \right|^2 df$$

- **Step 5:** Total noise power is sum of all contributions

$$\overline{v_{n_{TOTAL}}^2} = \sum_{j=1}^{N} \overline{v_{oj}^2}$$

Noise Budget

- Maximum SNR of a data converter:

$$SNR_{\max} = \frac{\overline{v_{u_{\max}}^2}}{\overline{v_{n_{TOTAL}}^2}}$$

Maximum input signal power

Total noise power

- The total noise power includes contributions from several sources:

$$\overline{v_{n_{TOTAL}}^2} = \overline{v_{n_q}^2} + \overline{v_{n_{sw}}^2} + \overline{v_{n_{OPAMP}}^2} + \overline{v_{n_{OTHER}}^2}$$

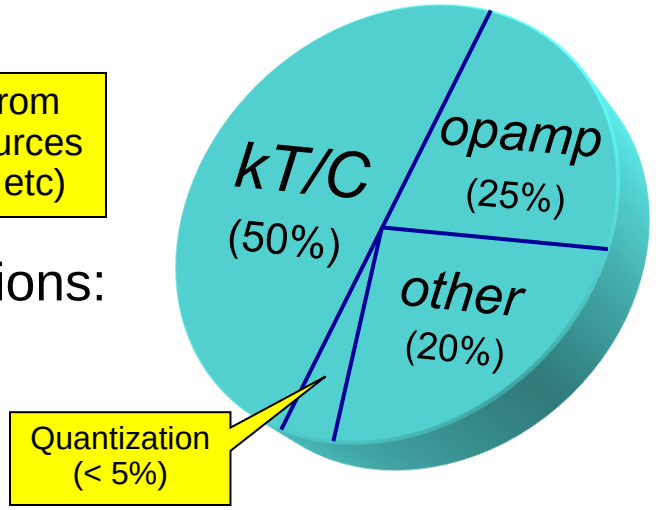
Quantization noise

Switch (kT/C) noise

Opamp thermal noise

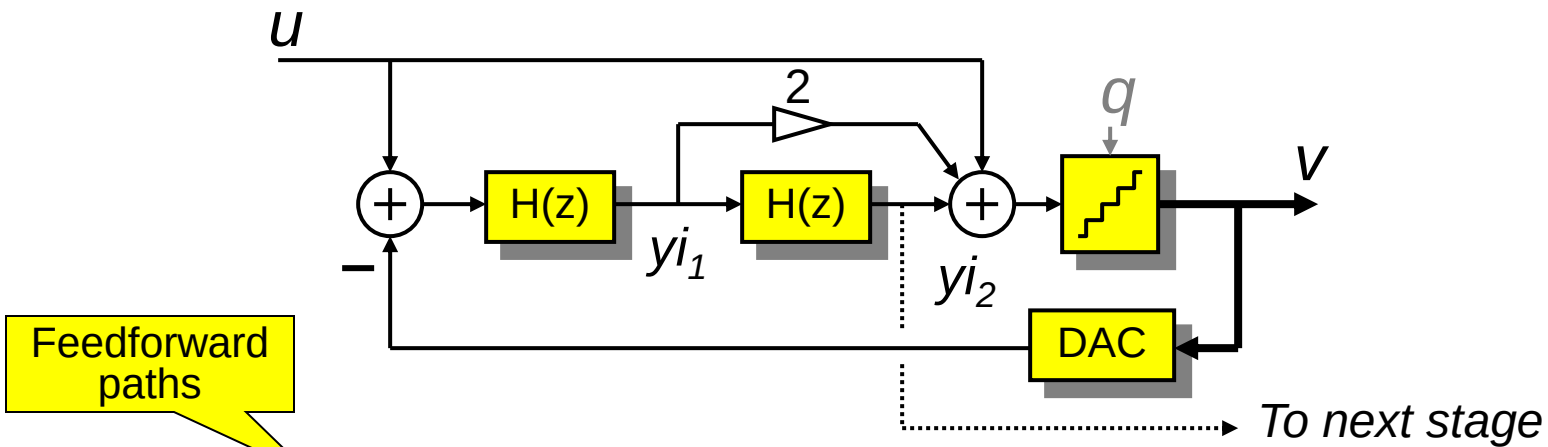
Noise from other sources (digital, etc)

- A good balance between these contributions:



Example: Low-Distortion ΔΣ Topology

- In conventional topologies, integrator nonlinearities are attenuated by loop. For low oversampling ratios, this is not effective.
- Distortion can be avoided by making STF = 1:



$$STF = \frac{1 + 2H + H^2}{1 + 2H + H^2} = 1 \qquad NTF = \frac{1}{1 + 2H + H^2} = \left(1 - z^{-1}\right)^2$$

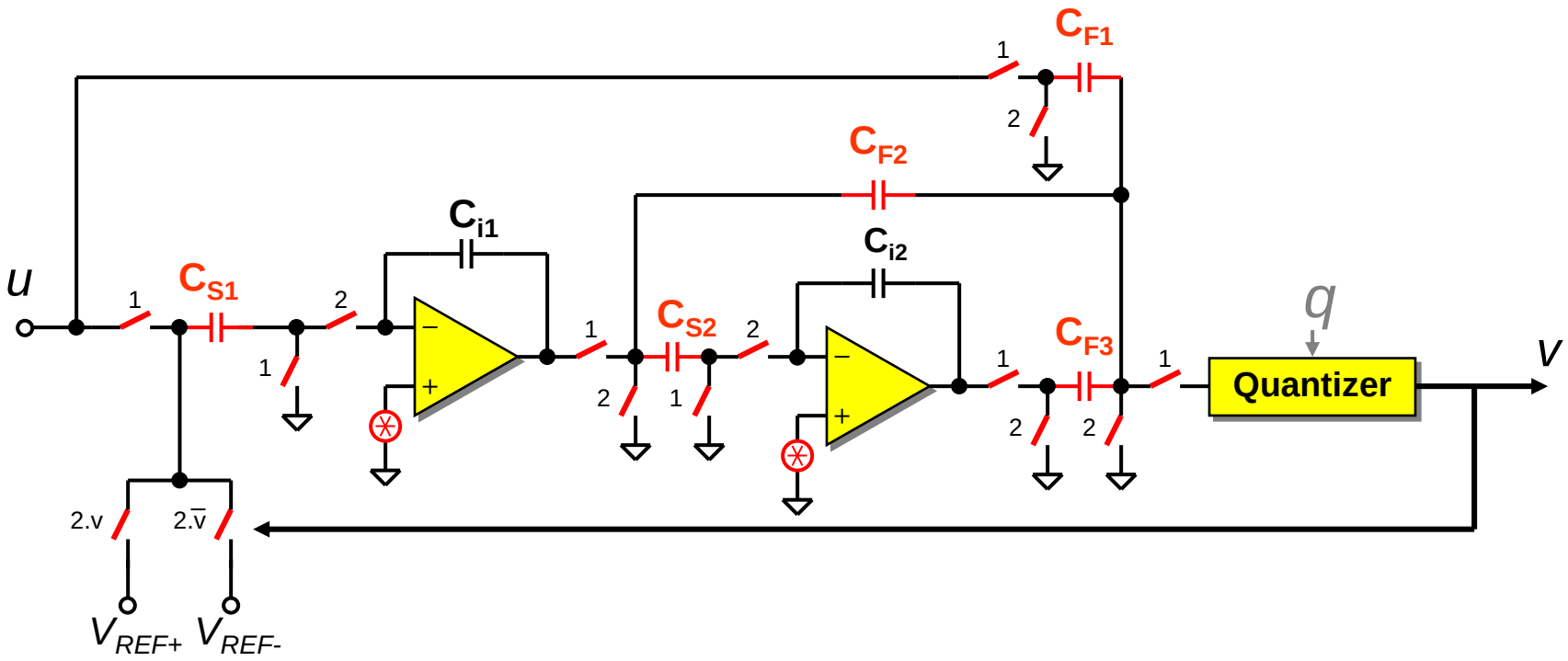
- Integrators do not process input signal, only quantization noise.

No signal ⇒ No distortion.

- For MASH structures, quantization noise can be tapped directly from y_{i2}.

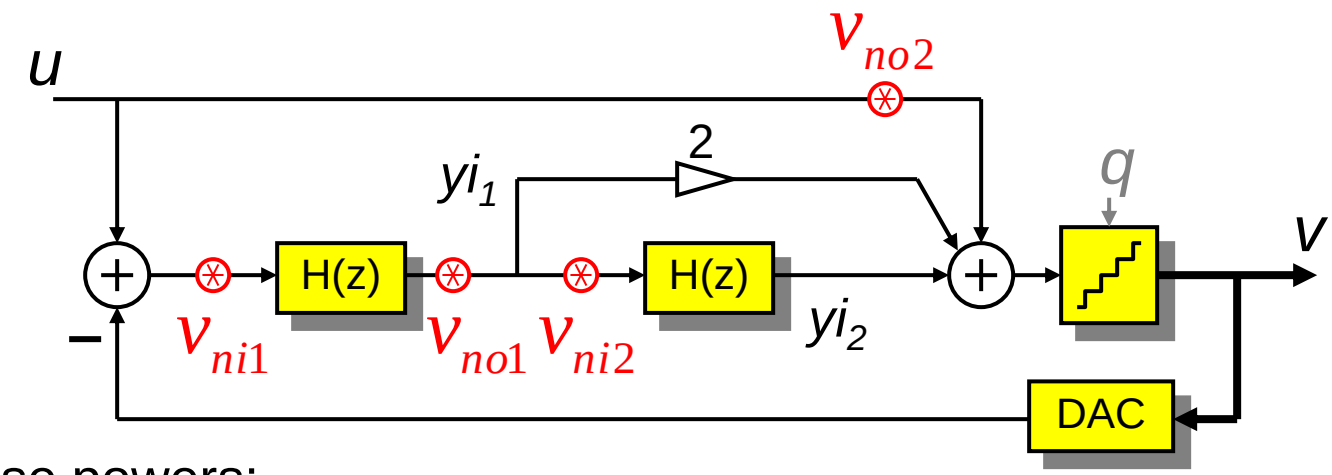
Noise Calculation Example (1)

- **Step 1:** Identify thermal noise sources in the topology:



Noise Calculation Example (2)

- **Step 2:** Calculate PSDs of noise sources:



- Noise powers:

$$\overline{v_{ni1}^2} = \frac{2kT}{C_{S1}} + \frac{kT/3C_{S1}}{x_1 + 1}$$

$$\overline{v_{no1}^2} = \frac{4kT}{3C_L}$$

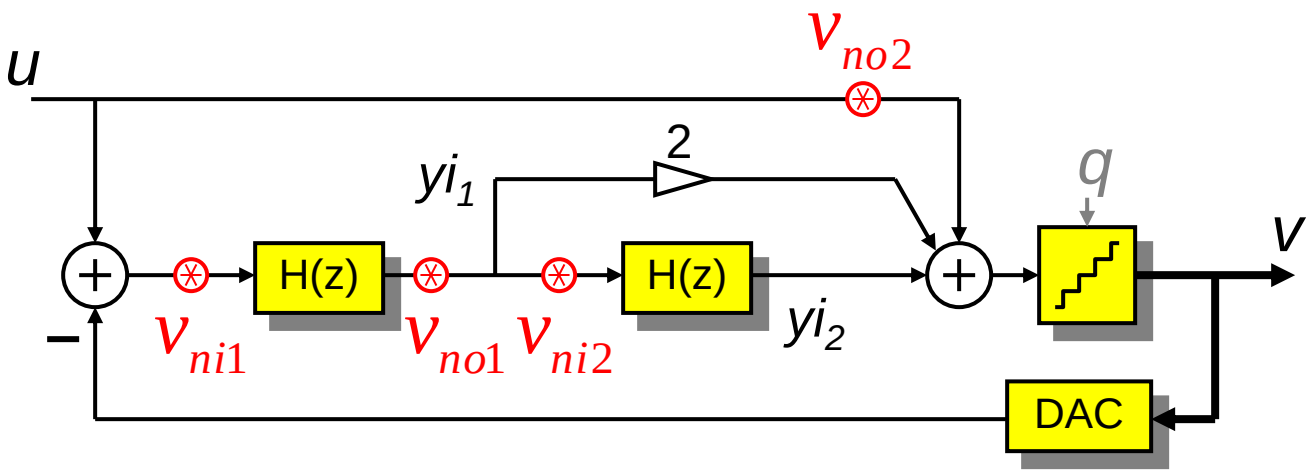
$$\overline{v_{ni2}^2} = \frac{2kT}{C_{S2}} + \frac{kT/3C_{S2}}{x_2 + 1}$$

$$\overline{v_{no2}^2} = 2kT\frac{(C_{F1} + C_{F2} + C_{F3})}{C_{F1}} + \frac{4kT}{3C_L}$$

- The PSDs are obtained by dividing noise powers by $f_s/2$.

Noise Calculation Example (3)

- **Step 3:** Calculate transfer function from each noise source to output:



- Assuming $H(z) = z^{-1}/(1 - z^{-1})$:

$$NTF_{i1}(z) = \frac{H^2 + 2H}{(1+H)^2} = 2z^{-1} - z^{-2}$$

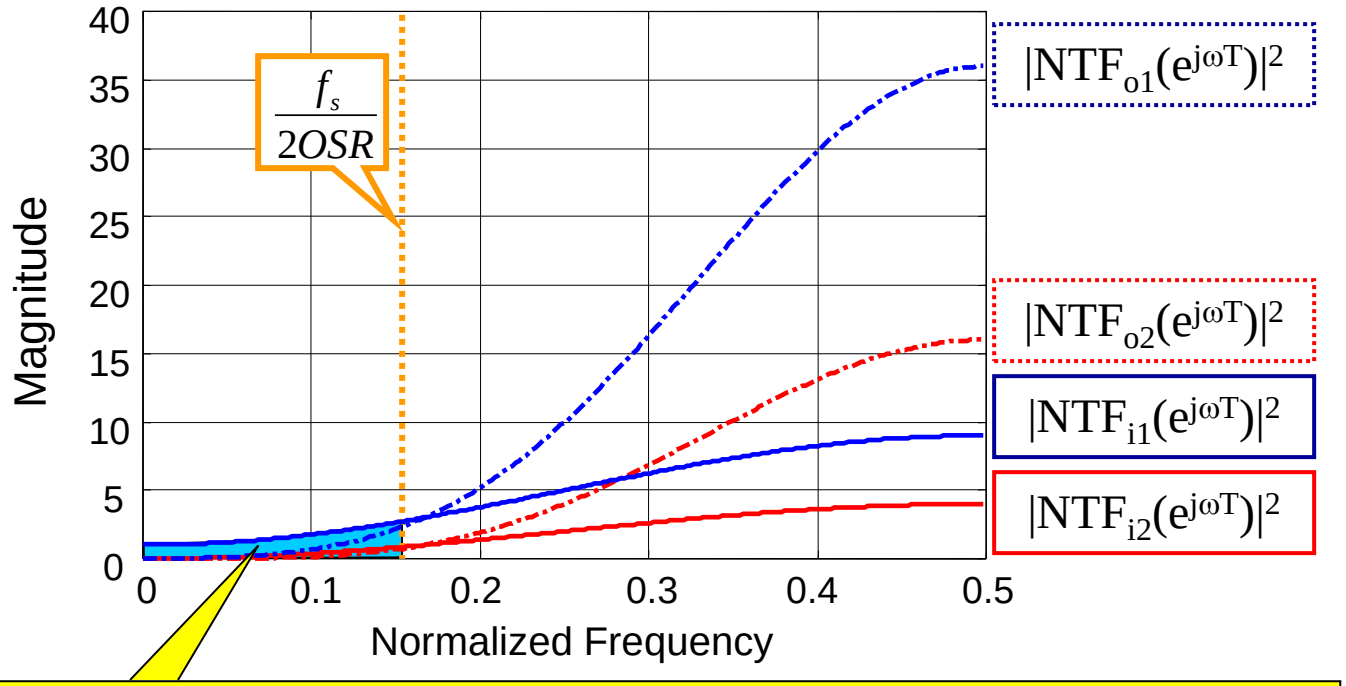
$$NTF_{o2}(z) = \frac{H+2}{(1+H)^2} = (1 - z^{-1})(2 - z^{-1})$$

$$NTF_{i2}(z) = \frac{H}{(1+H)^2} = z^{-1}(1 - z^{-1})$$

$$NTF_{o2}(z) = \frac{1}{(1+H)^2} = (1 - z^{-1})^2$$

Noise Calculation Example (4)

- **Step 4:** Integrate each noise PSD over desired bandwidth:



$$\overline{N_{i1}^2} = \frac{2\bar{v}_{ni1}^2}{f_s}\int_0^{\frac{f_s}{2OSR}} |NTF_{i1}|^2 df = \overline{v_{ni1}^2}\left[\frac{5}{OSR} - \frac{4}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right] \approx \frac{\overline{v_{ni1}^2}}{OSR}$$

(Tip: To save time, use a symbolic analysis tool such as Maple™)

Noise Calculation Example (5)

- Similarly:

$$\overline{N_{o1}^2} = \overline{v_{no1}^2}\left[\frac{14}{OSR} + \frac{4}{\pi}\cos\left(\frac{\pi}{OSR}\right)\sin\left(\frac{\pi}{OSR}\right) - \frac{18}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right] \approx \frac{\pi^2\overline{v_{no1}^2}}{3OSR^3}$$

$$\overline{N_{i2}^2} = \overline{v_{ni2}^2}\left[\frac{2}{OSR} - \frac{2}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right] \approx \frac{\pi^2\overline{v_{ni2}^2}}{3OSR^3}$$

$$\overline{N_{o2}^2} = \overline{v_{no2}^2}\left[\frac{6}{OSR} + \frac{2}{\pi}\sin\left(\frac{\pi}{OSR}\right)\cos\left(\frac{\pi}{OSR}\right) - \frac{8}{\pi}\sin\left(\frac{\pi}{OSR}\right)\right] \approx \frac{\pi^4\overline{v_{no2}^2}}{5OSR^5}$$

- **Step 5:** Finally, total noise is sum of all contributions:

$$\overline{N_{TOTAL}^2} = \overline{N_{i1}^2} + \overline{N_{o1}^2} + \overline{N_{i2}^2} + \overline{N_{o2}^2}$$

Numerical Example

- Assume the loop operates with OSR=256, and choose x=2. Then,

$$\overline{v_n^2} = 8.25 \times 10^{-3} \frac{kT}{C_{S1}} + 5.88 \times 10^{-7} \frac{kT}{C_{S2}} + 1.42 \times 10^{-10} \frac{kT}{C_{F1}}$$

- Since C_{s1} and C_{C1} dominate the noise performance, ignore the rest.
- Assume maximum input power is $0.25V^2$,and 16-bit noise performance is desired. Total allowed noise power:

$$\overline{N}_{total}^2 = 38 \times 10^{-12} V_{rms}^2$$

- Allocating 75% of total noise to the thermal noise:

$$C_{S1} \approx 8.25 \times 10^{-3} \frac{kT}{0.75 \cdot \overline{N_{TOTAL}^2}} \approx 1.2 \text{ pF}$$

Additional Considerations

- **Wideband operation (OSR < 16):**
  - Input stage does not dominate noise. Optimization algorithms should be used to minimize total capacitance while meeting the noise target.
- **Fully-differential circuits:**
  - Use same total capacitance as for single-ended circuit. Noise power increases by 3 dB for each side, and by 6 dB for differential mode. Signal power also increases by 6 dB, so total SNR is the same.
- **MASH topologies:**
  - Transfer functions should be calculated for whole system.
  - Quantization noise is cancelled, and so is the noise from some sources.
- **Calculations assume brick-wall decimation filter.**
  - For more accuracy, actual transfer function of the decimation block can be included in calculations.
- **|STF(f)| = 1 was assumed.**
  - Calculations are output referred. Signal power is affected by STF.

References

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[3] C. Enz and G.C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections," *Proceedings of the IEEE*, vol. 84, no. 11, Nov. 1996, pp. 1584-1614.

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[6] A.Heck, *Introduction to Maple*, Springer Verlag, 2003.

[7] K. Kundert, "Simulating switched-capacitor filters with SpectreRF," `http://www.designers-guide.com/Analysis/sc-filters.pdf`.

[8] G. C. Temes and J. Silva, "Simple and efficient noise estimation algorithm," *Electronics Letters*, vol. 40, no. 11, May 27, 2004, pp. 640-641.